THE DAC RESOLUTION ENHANCEMENT FOR DC APPLICATIONS BY USING MULTIPLE PWMS ON ATMEGA328

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Abstract: To gain higher analog output levels from digital systems, a high resolution DAC is required, which is usually a cost tradeoff. This research demonstrates an affordable way to increase the DAC resolution with a low cost microcontroller. It works by merging 3 PWM signals which are generated by an ATMEGA328 microcontroller in order to be used as an input into an RC digital to analog voltage converter. The merging is completed by using digital circuit, which produces a new carrier frequency by reducing the original PWM carrier frequency by a half. The new carrier frequency is merged with 2 PWM signals by logical operation. The theories and experiment results reveal that converting the united PWM signal to analog voltages is possible. The conversion outcome is the improvement in analog voltage output resolution when compared to the conversion from a single PWM.

Keywords: ATMEGA328, Microcontroller, Digital to Analog Converter, DAC, PWM, Resolution

1. INTRODUCTION

PWM signals play an important role in control systems and commonly used in several control systems such as power electronics [1], speed controllers [2], and digital to analog voltage converters [3]. In digital to analog conversion, the resulting analog signal is mainly used in applications such as digital audio devices [4] and in data communication between controllers and measurement devices. One of a low complexity conventional conversions is, delivering a single PWM signal through a frequency filter which cut out a certain PWM carrier frequency. The outcome signal is analog voltage whose value depends on the PWM duty cycle value.

The ATMEGA328 microcontroller is capable of generating several PWM signals concurrently [5], which contain the same carrier frequency and independently specified duty cycle value. The value can be adjusted from 0-100 percent by specifying a particular value in a timer register, where the numbers are limited by the size of the built-in microcontroller's timer. Therefore, when the PWM signal is converted into an analog voltage signal, the output analog voltage level, which is known as resolution, is also limited.

A higher analog voltage control resolution means greater controller ability for voltage adjustment in a narrower gap. This adjustment ability clearly impacts the efficiency of a particular signal generation [6] and also affects the quantity of data represented by analog voltage levels. There are numerous ways to improve the digital-to-analog resolution which was introduced such as the combined Sigma-Delta and PWM interpolation technique [7] which gives a high performance result and low analog complexity. However, the overall implementation of this technique still requires many connections and elements and also some comprehensive mathematics. Another example is Dithered Output DAC which its theory is quick and periodic writing two or more different digital values to a DAC and filters the DAC output, and then the DAC output value becomes the average of the digital values written to the DAC [8]. The latter concept is simple but may make greater demands on a controller's computation time and resources.

To achieve higher resolution without running complex software computations and costly hardware units, this research offers a new approach by developing a few digital components to merge 3 generated PWM signals which come from a single microcontroller, ATMEGA328, so as to extend the duty cycle step numbers and diminish the intervals of adjacent analog voltage output values from the frequency filter.

2. BACKGROUND AND THEORIES

2.1. PWM

A PWM or Pulse Width Modulation signal is introduced as a constant frequency square wave. This frequency is called a carrier frequency. The PWM signal has 2 constant amplitude levels which is either V_{on} or V_{off} as described in Fig. 1.

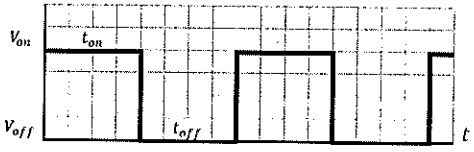


Fig. 1. The PWM signal with 50% duty cycle

can be different within 256 steps. Therefore, the analog voltage levels are within 256 steps either. These 256 steps may not be sufficient to provide good controllability for some devices. Expanding these steps with a simple way comes up by realizing that in some applications, they do not require many PWM channels to be operated so some are vacant as seen in Fig. 3.

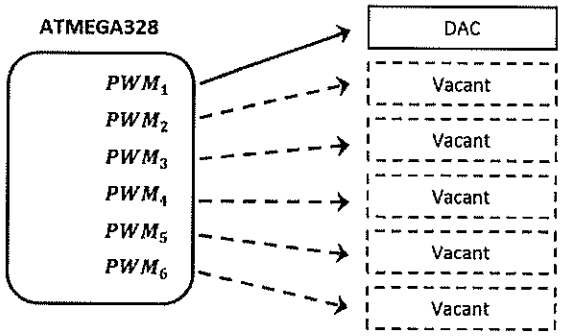


Fig. 3. Six PWM signals produced from a single ATMEGA328; one is occupied, the rest are available

An idea is making the most of the remaining PWM vacant channels by taking two more PWM channels, PWM_2 and PWM_3, joining them with PWM_1 to construct PWM_Z which increases the number of duty cycle setting steps. This new process is described in Fig. 4. It contributes the PWM_3 as a frequency divider input frequency, which is then divided by half to be a new carrier frequency Q and its inverse $\overline{Q}$. To form PWM_Z, the PWM_1, PWM_2, Q and $\overline{Q}$ are united by logical operation. The resulting PWM_Z is converted to an analog voltage signal by a RC frequency filter.

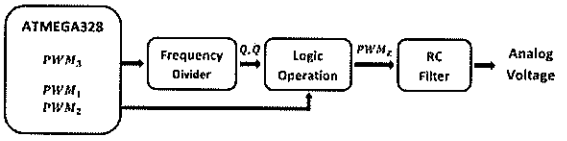


Fig. 4. Block Diagram of PWM to analog converting process

The frequency divider circuit is generally implemented by a D-Flip Flop [15]. The Boolean expression of the logical operation which forms PWM_Z is described in (3). It sums two comparison results together. The first one is between PWM_1 and Q, and the second one is between PWM_2 and $\overline{Q}$. The signal timing relation of (3) is shown in Fig. 5.

$$PWM_Z = PWM_1 Q + PWM_2 \overline{Q} \qquad (3)$$

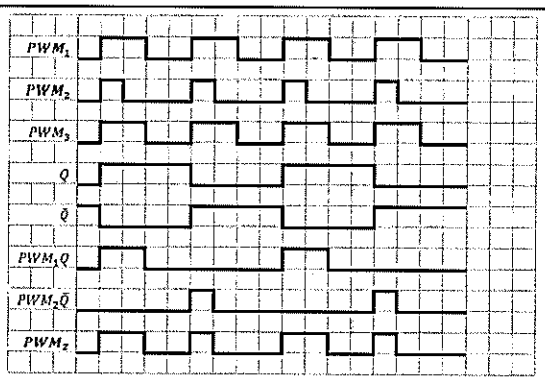


Fig. 5. Signal timing relationships according to (3)

Deriving (3) by applying the DeMorgan's Theorem [16] will obtain its multiplication form, that is (4). The frequency divider and the signal multiplication forms in (4) are schematically connected by the digital logic gates, shown in Fig. 6.

$$PWM_Z = \overline{\overline{PWM_1 Q} \cdot \overline{PWM_2 \overline{Q}}} \qquad (4)$$

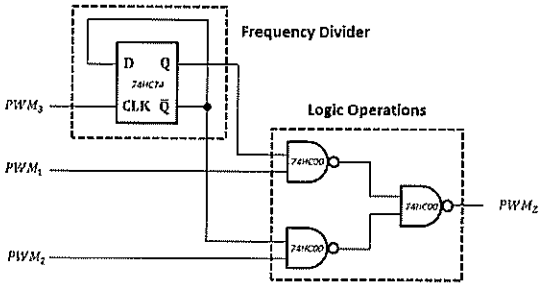
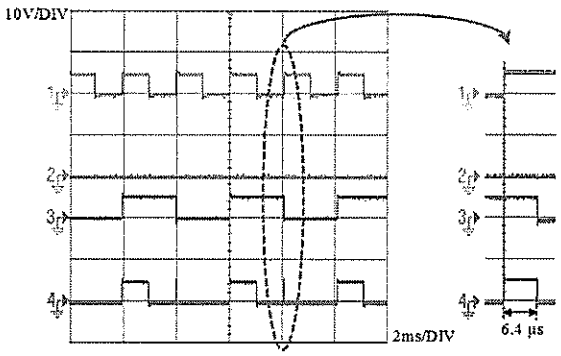


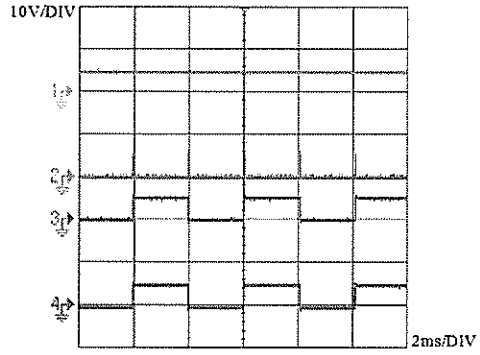
Fig. 6. The digital logic diagram of (4) to unite 3 PWM signals

4. EXPERIMENTAL SETUP

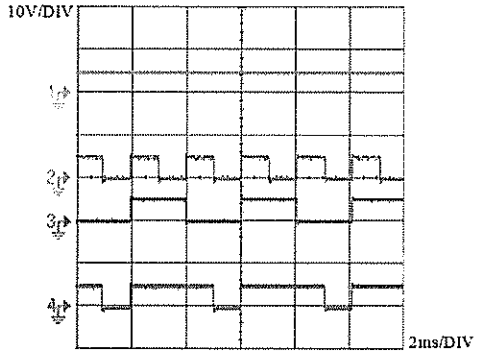
All implemented circuit elements are supplied by the external voltage regulator. All VCC supplies are 4.968 V. The ATMEGA328 application board, shown in Fig. 7, reads the input signals from two delicate push buttons connected to the D12 and D13 channels to recognize the increasing or decreasing PWM_Z duty cycle specification. The push button BT_{up} is for an increasing signal and BT_{dn} is for a decreasing signal. To form the PWM shape of PWM_Z, the programming algorithm in Fig. 8 is developed and is running inside the ATMEGA328. The algorithm interprets the recognized PWM_Z duty cycle value to the particular PWM_1, PWM_2 and PWM_3 duty cycle value. These values are transferred to a PC for monitoring and are used inside the ATMEGA328 for PWM production. The three generated PWM signals are transferred to the next implemented circuits via the D9 D10 and D11



(a)



(b)



(c)

Fig. 12. The oscilloscope channels 1 to 4 are connected to PWM_1, PWM_2, Q and PWM_Z in order respectively. The scales are set to 10V/DIV vertical and 2ms/DIV horizontal. In (a) The PWM_Z duty cycle value is 128, the algorithm creates the PWM_1 and the PWM_2 duty cycle values are 128 and 0 respectively In (b) the PWM_Z duty cycle value is 256, the algorithm creates the PWM_1 and the PWM_2 duty cycle values are 255 and 1 respectively. In (c) the PWM_Z duty cycle value is 383, the algorithm creates PWM_1 and the PWM_2 duty cycle values are 255 and 128 respectively.

5. RESULTS AND DISCUSSION

To examine the invented merging circuit operation and algorithm, the example of PWM_Z duty cycle values are set. They are within 3 intervals; less than 256, equal to 256 and greater than 256. Each setting duty cycle value creates its own individual PWM_1, PWM_2, Q and PWM_Z which are captured by an oscilloscope as shown in Fig. 12(a), (b) and (c). All signals act according to the merging concept. The PWM_Z is clearly the result of the combination of the 4 signals explained in (3). The small time delay between the output and input of 74HC74 makes produced Q shifts from both PWM_1 and PWM_2 for 6.4 µs. The effect of this signal shift is clearly seen when the PWM_Z duty cycle value is less than 256, where there is a spike that develops in every period as shown in the dash ellipse in Fig. 12(a). This spike makes the PWM_Z frame not look perfectly alike to a typical PWM but it eventually takes no effect to the analog voltage output value since it is eliminated by the serried RC frequency filter in Fig. 10.

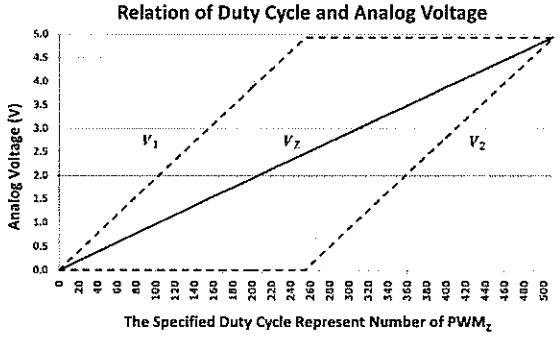


Fig. 13. The analog voltage V_1, V_2 and V_Z varies according to the PWM_Z duty cycle adjustment from integer number 0 to 510

In order to observe the variation of analog voltage values V_1, V_2 and V_Z, the PWM_Z duty cycle value is re-specified. Let it begin from integer number 0 (0% duty cycle) and increasing one step at a time to the final value at 510 (100% duty cycle). The resulting analog voltage from the RC frequency filters are measured by multi-meters as shown in Fig. 13. The solid line V_Z is gradually increasing along with the growth of the PWM_Z duty cycle value. It begins from 0 V minimum value to 4.936 V maximum value. The result reveals that the analog voltage values relate to the PWM_Z specified duty cycle value, they are direct variation and one to one function. The interval of analog voltage V_Z when the